Brd2 report

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ECEN5730

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**Introduction/theory:**

The purpose of this board was to demonstrate the impact design best practices has on switching noise on two identical circuits. To demonstrate this, a 555 timer was connected to two hex inverter chips. For both chips, the inputs of three of the inverters were connected to the 555 timer, and had their outputs connected to indicator LEDs in series with 50Ω resistors. Two of the inverters were connected in quiet high and quiet low configurations. A quiet high configuration is used as a test point for noise in a circuit, the inverter had its input connected to ground, and its output connected to a test point. A quiet low configuration is used in a similar manner, except its input is connected 3.3v. With both inverter chips connected in this way, one was designed with bad design practices, and the other with best practices.

The bad design had its chip’s decoupling capacitor further away from its VCC connection. During the PCB layout and routing process, the ground plane was also removed for the bad design.

The reason why a ground plane is added into a circuit to reduce noise is because by having a ground plane, current will travel from power to ground in the path of least impedance. This means that whatever path on the ground plane results in the least resistance, current will automatically pick that path. But if the ground path is routed in a long winding trace, this can increase the power to ground path length, which increases noise. This is because the amount of mutual inductance on a wire is determined by its wire length, as seen in the following equation:

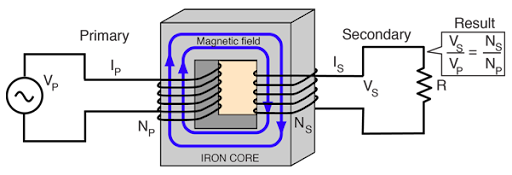


Figure , Mutual inductance illustration

* Fig1 demonstrates that return path length, or N is proportional to the induced voltage, V.

Here we can see the number of windings in a coil, is proportional to the induced voltage on adjacent coils. This is also why the decoupling capacitor should be placed closer to an IC for less noise, it reduces the power to ground path. A decoupling capacitor supplies current at a closer location than the main current source of the board, therefore it has a lower inductive path, and decouples from the board’s PDN.

When measuring the signals in this board, they are compared to the measurements collected from another reference board provided by the lab instructors.

**Equipment/components/BOM:**

The following components and equipment was used in the production of this board.

COMPONENTS:

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Figure , Equipment used

* Fig2 contains the part numbers are quantity of all the components used in this board.

BENCH/TEST EQUIPMENT:

1xBench oscilloscope  
2xoscilloscope probes  
1xlaptop running Altium.  
Various conductors.

**Potential risk sites:**

There are many potential risk sites for this board, for one is the close proximity of the switches to other components in the board. If I ever need to re-solder any connections on this board, and the switches are already soldered on the board, then I would need to detach the switches. The same goes for every other component as well, but the components which really stick out have the highest risk of this happening.

 Another risk site is accidentally using the wrong capacitors when soldering the board together. To avoid this issue, I will have my laptop open with reference documents while I solder, to ensure everything will be soldered with the proper components.

In addition, another thing that could go wrong is that I could accidentally burn out my eyes with splashes of stray solder when soldering. One way to avoid this is to wear safety goggles while soldering.   
  
Another thing that could go wrong is that I solder the IC's upside down. I will also have reference documents pulled up while I solder to combat this, and make sure the chip orientation matches that found online.

**POR/General expectations of board:**

In the power block of the board, 5v should be being produced by the barrel jack adapter. Moreover, the output of the LDO should be 3.3v, and the output of the LDO should not have significant noise disruption. In the timer block, the output signal of the 555 timer should have an amplitude of 5v. The signal should have a duty cycle of 50%, and should oscillate at a frequency of 500hz. In the good and bad design inverter blocks, the 555 timer signal routed into both inverter blocks should produce an inverted version of the 555 timer output signal. Moreover, the quiet low and high signals on both design blocks should be an inverted version of its respective input signal. The switching noise observed on the bad design block on these victim lines should be higher than that of the good design block. In general, all components of the PCB should be electrically connected where intended.

**Schematic sketch:**

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Figure , Sketch of the power block

* In fig 3, the block powers the board and provides the backup 3v line via an LDO

**A diagram of a circuit

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Figure , sketch of the 555-timer block

* In fig 4, this block generates a 5v, 505hz square wave signal with a 66% Duty cycle

**A diagram of a circuit

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Figure , sketch of the good design block

* In Fig5, the good design block is designed so that the decoupling capacitor is close to the power pin, reducing noise.

**A diagram of a circuit

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Figure , sketch of the bad design block

* In Fig 6, the bad design block is designed so that the decoupling capacitor is further away from the power pin, increasing signal noise

**Altium schematic:**

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Figure , Overall schematic

* In Fig 7, the overall design of the board can be seen.

Everything to the left of the LDO component in the power block was reused. Information about the reused circuitry can be found in my brd1 [report](https://github.com/O11WL1D/ECEN3730_PCBS/blob/master/BRD1/brd1%20report%20.docx). The LDO or Low drop out chip converts the 5v coming from the barrel jack adapter and converts it to 3.3v. Inside of the LDO is a feedback circuit which checks what the circuit’s output voltage is. If this voltage is higher or lower than 3.3v, the LDO adjusts the resistance of an internal MOSFET transistor in order to keep the output at 3.3v. This feedback loop between the LDO’s input and output can lead to oscillation on its output if there is ever noise on the output line. To combat this, a filter capacitor is added to the output line of the LDO.

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Figure , Power conditioning block close up

* For the timer block I copied the design I used for my first board. Information about this block can be found in my brd1 [report](https://github.com/O11WL1D/ECEN3730_PCBS/blob/master/BRD1/brd1%20report%20.docx).

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Figure , Timer block closeup

This design is re-used for the bad design block, with the exception of the decoupling capacitor being closer to the hex inverter chip. Here you can see the timer output is connected in the way described in the report introduction. The 3.3v line from the LDO is also seen connected to the output of the 555 timer. This is used to supplement the 5v 555 output signal if it ever experiences noise in the circuit. When two voltage sources are attached in parallel, the voltage across each source is the same as the highest voltage source present. This means that the voltage is dictated by the 5v timer output until it dips to 3.3v, which at that point the voltage on the line is 3.3v. If the 5v timer output dips lower than 3.3 volts or is grounded, all of the voltage should be dropped across r5.

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Figure , Good design Indicator block closeup

A diagram of a circuit

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Figure , bad design Indicator block closeup

**Altium PCB layout/routing:**

As you can see in the image below, the ground plane on the bad design (lower bottom left) is selectively removed to amplify the effects of noise on the circuit. Moreover, c6 the decoupling capacitor was moved away from the hex inverter to reduce its effectiveness.

**A blue circuit board with red and blue text

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Figure , Overall PCB design of brd2

* In fig 12, the bad design does not have a ground plane, and has its decoupling cap further away, whereas the good design has opposite features.

**Unassembled board:**

**A green circuit board with many small holes

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Figure , The unassembled PCB

**Assembled board:**

**A green circuit board with red lights

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Figure , The assembled PCB with the good design block powered on

**Reference board:**

**A green circuit board with many small chips

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Figure , Course reference board results are compared to

* In Fig 15, it can be seen that the bad design features include a faraway decoupling capacitor and a missing ground plane.

**Scope captures:**

**Power block:**

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Figure , measurement from 5v powerline

* In Fig 16, the yellow line measures the 5v powerline, which was found to be 5.1v. This is exactly the desired voltage outlined in the POR.

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Figure , 3.3v being read on the 3v powerline.

* In the figure above, 3.3v was read on the 3v powerline. This matches the desired voltage in the POR.

**Timer block:**

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Figure , 555 timer output, 5v, 505hz, 60% duty cycle.

* In fig 18, most attributes were close enough to their desired values in the POR. Further analysis on means of increasing prototype signal accuracy can be found at the end of this report.

**Good design block:**

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Figure , quiet high signal on good design block (Green), 555 output is yellow, noise has max amplitude of 200mv

* In fig 19, the max amplitude is 200mv, which is significantly lower than that on the bad design block, 1500mv

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Figure , 555 inverter on good design block, yellow is the 555 timer input, green is the inverter output.

* In Fig 20, the input 555 signal is being inverted with the exact same amplitude, frequency and duty cycle measurements. This matches the outlined expectations in the POR.

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Figure , quiet low signal on good design block (Green), 555 output is yellow, max noise amplitude is 100mv

* In Figure 21, the qlow noise on the good design block is lower than that of the bad design block, which is 120mv. This could be higher, which is discussed later in the report.

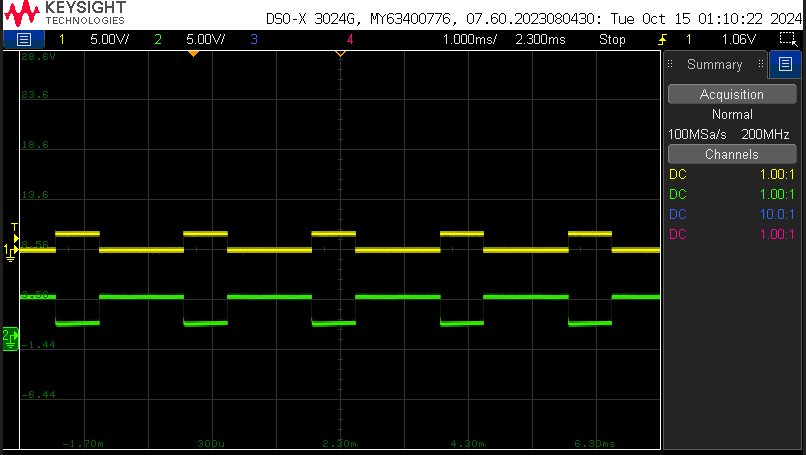


Figure , 50 Ω sense resistor on quiet good design block (green), 555 output is yellow ,0.03A current draw, 1.5v drop.

* In Fig 22, all values on the sense resistor are nominal, the LEDS on both blocks were a little bright so next board will need to feature higher sense resistor values.

**Bad design block:**

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Figure , 555 inverted output (Green), yellow is 555 output, on bad design block

* In fig 23, the inverted output matches all characteristics of the 555 timer output, with the exception of being inverted.

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Figure , Sense resistor output(green), yellow is 555 timer out, on bad design block. 0.029A current draw, 1.47V drop.

* In Fig 24, the values of the current draw and voltage drop are pretty much the same as in the good design block.

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Figure , quiet low signal on bad design block(Green), yellow is 555 timer out, max noise amplitude is 120mv

* The qlow noise on the bad design block is higher than that in the good design block, here it is 120mv, but in the good design block it is only 100mv

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Figure , quiet high signal on bad design block(green), yellow is 555 timer out, noise max amplitude is 1500mv

* Here the qhigh noise on the bad design block is significantly higher than that on the good design block, here it is 1500mv whereas its only 200mv on the good design block.

**Class reference board measurements:**

**Power block:**

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Figure , 3v signal reading on power block of ref board.

* Nominal values observed on the class board.

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Figure , 5v reading on ref board

* Nominal values observed on the class board.

**Timer block:**

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Figure , Reading from the timer block on the ref board, 1000hz, 60% duty cycle, 5v

* In fig 29, the timer only differed from my board in the fact that it is 494.9hz higher than mine.

**Ref board good design block:**

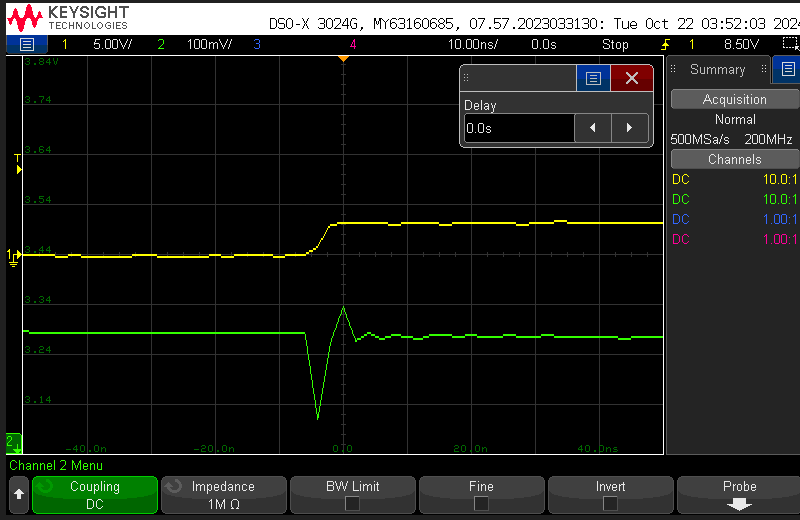
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Figure , qhigh signal on gbd ref board(Green), Yellow is 555 out, Max noise amplitude is 180mv

* In Fig 30, the noise is 20mv lower than my board. This indicates that better design principles still could have been utilized to produce a higher quality board.

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Figure , qlow on gdb ref board(green), yellow is 555 timer output, max noise amplitude is 20mv.

* The max noise amplitude in fig21 is 80 mv lower than my board’s good design block. Another indication of my board’s imperfections.

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Figure , 555 inverter, ref board GDB output, yellow is 555 out, green is inverted signal.

* This signal is 500hz higher than my GDB, but otherwise the same as my board.

**Ref board bad design - no ground plane/ decoupling capacitor far away - :**

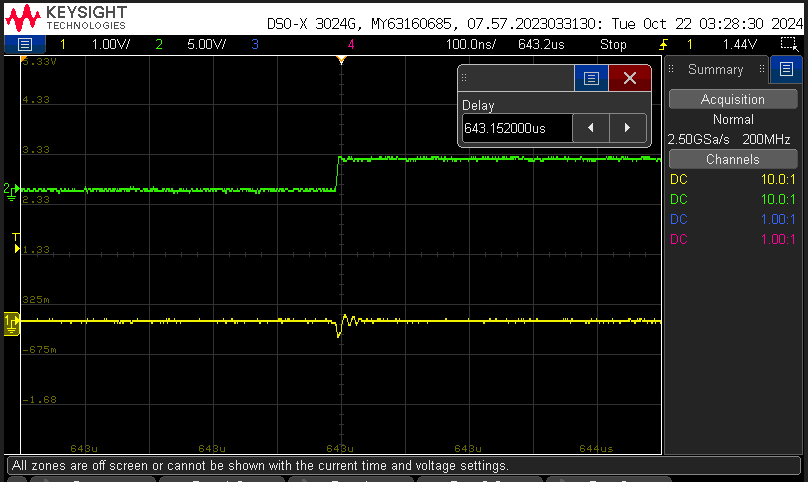


Figure , BDB no ground plane/ decoupling capacitor far away, noise is yellow, qlow amp =1200mv

* This noise is 1080mv lower than the BDB on my board.

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Figure , BDB no ground plane/ decoupling capacitor far away, noise is green, 555 out yellow- qhigh noise amp = 440mv

* The noise on this section is 1069mv lower than that on my board.

**Ref board bad design -> decoupling capacitor far away / ground plane present:**

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Figure , BDB decoupling capacitor far away / ground plane present, Noise is green, 555 out is yellow, qhigh noise amp= 300 mv.

* In the figure, the noise is -1200mv lower than that of my board. Maybe increasing the capacitance of my decoupling capacitors would have fixed this.

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Figure , BDB decoupling capacitor far away / ground plane present, Noise is green, 555 out is yellow, qlow max noise amp= 32 mv.

* In fig 36, the noise is 88mv lower than that in my board.

**DATA/POR fulfillment:**

It should be noted that the POR document started as a test characterization plan that I just added to. I would attach that plan, but that would be redundant.

**Power budget estimates/data:**

It should be noted that I could not find good information on the power consumption of the 555 timer, it just said that it was usually less than 1mw. Moreover, I couldn’t find anything on the hex inverter chip itself, which leads me to assume the power draw is negligible.

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Figure , Power consumption of the good and bad inverter blocks

* In fig 37, the power consumption seems to be reasonable for this kind of circuit.

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Figure , Power consumption of the timer and power blocks

* The power consumption here also seems to be a nominal value.

**Brd2 data:**

Here are measurements taken from all blocks, along with a table of POR satisfaction:

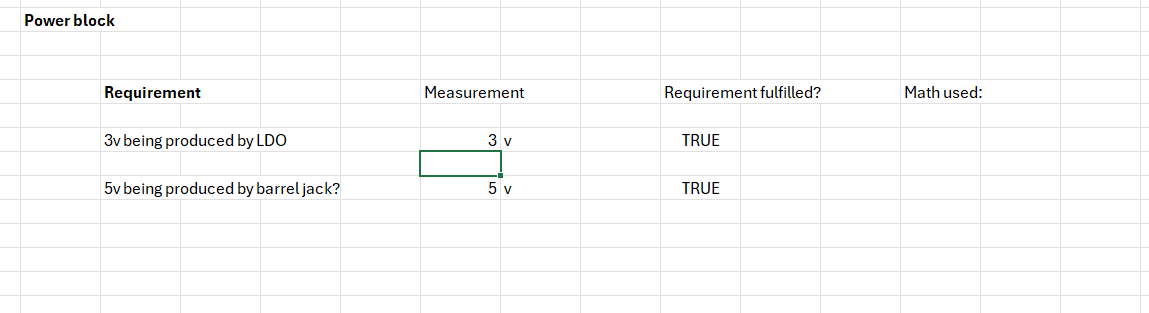


Figure , power block data and POR satisfaction

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Figure , Timer block data and POR satisfaction

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Figure , good design block data and POR satisfaction

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Figure , bad design block data and POR satisfaction

**Ref board data:**

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Figure , Ref board power block data

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Figure , ref board timer block data

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Figure , ref board good design block data

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Figure , ref board bad design – no ground plane + decoupling cap far away data

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Figure , ref board bad design – ground plane present + decoupling cap far away data

**Analysis:**

**Measurement analysis:**

The noise generated from the good design block is significantly less than the noise generate by the bad design block. The rise time of the bad design block was also longer than the good design block. This might be because with longer power to ground paths the rc time constant is larger, resulting in longer rise times. This demonstrates the importance of best design practices, such as adding in a ground plane and reducing dcc distance from power pins.

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Figure , quiet high and low good/bad block differences

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Figure , good/bad block rise time differences

**What worked well/ways to improve:**

When I first designed brd2 I arranged all of the components in a way that was ascetically pleasing, but when I began the routing process I realized that if the components were arranged in that manner it would be difficult to route the connections where they needed to go without adding in a significant number of vias and cross-under connections, thereby increasing board noise and degrading performance. Upon realizing this, I re-did the design for the afflicted sections. I instead placed the components closest to where they would be connected, which greatly reduced the number of vias in my design.

In future designs, when placing the components I plan to arrange things based on what results in the shortest paths between components.

During the assembly process, initially the 555 timer didn’t output a signal after I had soldered all of the components to the board. Upon inspection, I realized that the soldering iron I’d used was of a wider diameter than other irons in the lab. This made some of the connections difficult to make, and had resulted in a poor solder joint on the vcc connection of the 555 timer. To remedy this, I used the smaller soldering iron. Usage of a smaller soldering iron is something I plan to continue in future designs.

Moreover, the duty cycle of the timer is 15% higher than what was anticipated. I am sure that with higher quality control of the resistors used, this error could be reduced. A potential way to fix this issue in the future is to establish a tolerance range of acceptable component variation, and to reject any component which does not fall within that range.

**Class vs brd2 differences:**

I notice that most of the noise on the good and bad blocks of the ref board has a higher amount of noise than that on the good and bad blocks on my board. This result is somewhat surprising since my board is smaller than the reference board, but upon further investigation I realized that in my design file the power trace widths had been set to 15mil rather than 20mil. Wider trace widths generally tend to reduce noise, so maybe this is the cause for the variation.

This may be also be due to external factors contributing to the noise of the circuit. If any of my pins had a poor solder connection to the test point, i.e. low contact, that would increase the resistance of the trace, thereby altering the measured noise. With more time I would be able to check the connections and troubleshoot the signal noise further.

The difference between key figures can be found in the data section of this report.

**Conclusion:**

This board demonstrated the importance of best design practices while developing PCBS. By not including a ground plane, or by having significant distance between power pins and their decoupling capacitors, noise can be introduced into a circuit. Moreover, this board also demonstrated the importance of component verification during the assembly process. During the design of this board, the value of strategic component placement was also made apparent. Surely the principles and concepts taught in the creation of this board will enrich the design process of future boards.